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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/300,540	04/27/1999	LUKAS P. P. P. VAN GINNEKEN	54355	4583

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EXAMINER
KIK, PHALLAKA

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/300,540	VAN GINNEKEN ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-47* is/are pending in the application.

4a) Of the above claim(s) *31-47* is/are withdrawn from consideration. (claim 22 cancelled)

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *31-47* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. This Office Action responds to Applicant's amendment filed 10/15/2001. Claims 1-21,23-47 are pending, wherein claims 21 has been amended, claim 22 has been canceled, and claims 31-47 have been newly added. Claims 1-47 have been examined. As per claims 1-21,23-30, Applicant's arguments are not persuasive; therefore the previous Office Action is incorporated herein. New claims 31-47 are withdrawn from consideration as being directed to non-elected invention as given below.

Election/Restrictions

2. Newly submitted claims 31-47 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 31-47 are directed to a method for storing data for use by an automated logic design system comprising the steps which are distinctly different from the data structure containing the data model stored in the computer readable medium of **claims 21,23-30** and used in the method of digital circuit development of **claims 1-20**.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 31-47 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

3. The drawings filed on 4/27/1997 are acceptable under the new rules as being easily readable and scannable, as indicated in the previous Office Action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-6,14-20** are rejected under 35 U.S.C. 102(b) as being anticipated by **Rostoker et al.** (US Patent No. 5,541,849).

Rostoker et al. disclose a method and system for creating and validating low level description of electronic design from higher level behavior-oriented description, including estimation and comparison of timing parameters (abstract).

As per **claims 1-2,19-20,** all of the elements of the claims are illustrated in Fig. 9 (see also col. 9, line 60 to col. 12, line 22 and Fig. 12), wherein the electrical signals are generated by the VHDL compiler and simulator and design partitioner (blocks 904 and 908) (Steps 2-6) producing module description (step 7), logic synthesis is performed in blocks 912,916,910,918, and the physical placement is performed in blocks 920 and 922, and VHDL is a form of the hardware description language description, wherein the partitioning and composition steps (steps 3 and 5) provide for the retrieving a portion of the data model corresponding to the physical area while not retrieving portions of the

data model not corresponding to the physical area and wherein the formal verification or validation (part of steps 3 and 6, col. 10, lines 10-21 and 34-54) must of necessity copy the data model to be used for formal verification so that the original library models are not modified.

As per **claims 3-6,14-16,** the data model being a hierarchy of data objects having various objects attributes are described in col. 10, lines 4-28 (see also col. 15, line 48 to col. 17, line 5), wherein the objects having functional equivalents are inherently included as part of the components in the library having the same function but different optimization criteria (i.e., higher speed or less area or more drive ability) as is common in the art.

As per **claims 17-18**, the common tool including a timing simulator is also described in col. 11, lines 47-55, 64 to col. 12, line 9.

6. **Claims 21,23-30** are rejected under 35 U.S.C. 102(b) as being anticipated by **Mahmood et al.** (US Patent No. 5,726,902).

Mahmood et al. disclose a method and apparatus for characterizing the timing behavior of datapath in integrated circuit design and fabrication, having an architecture library for representing digital circuits (abstract).

As per **claims 21,24-26**, all of the elements in the claims are taught in Table 1, Table 2 and Table 4 containing both logical and physical parameters (see also col. 10, line 57 to col. 11, line 42; col. 11, line 8 to col. 12, line 43, and col. 13, line 66 to col. 14, line 61), wherein the datapath cell instance generated in netlist corresponds to the generated data model.

As per **claim 23**, the library including technology library and circuit library is also described in col. 16, lines 12-38.

As per **claim 27**, the plurality of cells having primitive cell and non-primitive cell is also described in col. 11, lines 31-42.

As per **claims 28-30**, since it is not clear from Applicant's specification what the KD tree data structure is, the tree expression as described in col. 6, line 46 to col. 7, line 26 meets these further limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 7-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rostoker et al.** (US Patent No. 5,541,849) in view of **Mahmood et al.** (US Patent No. 5,726,902).

As per **claims 7-13**, **Rostoker et al.** disclose all of the elements of claims 1 and 4 as discussed in the rejection of claims 1 and 4 above from which the claims depend but failed to specifically disclosed the KID tree data structured implementation. Such tree data structured is taught by **Mahmood et al.** used for optimally synthesizing an IC from HDL description (abstract; col. 6, line 46 to col. 7, line 26; col. 1, lines 50-62) wherein since it is not clear from Applicant's specification what the KD tree data structure is, the tree expression as described in col. 6, line 46 to col. 7, line 26 meets these further limitations. It would have been obvious to one of ordinary skilled in the art

at the time of the invention to further incorporate the tree data structured implementation of the data model library as taught by **Mahmood et al.** to the method/system of **Rostoker et al.** because such tree data structured method optimally synthesize an IC from an HDL specification.

Remarks

9. The rejection of **claims 21,23-30** under 35 U.S.C. 101 are withdrawn in light of the amendment filed 10/15/2001 which provide sufficient utility to the data structure as claimed.

10. As per **claims 1-20**, Applicant argued that **Rostoker et al.** failed to teach using "a data model" that contains parameters that include both logical and physical parameters of the circuit. The Examiner is not persuaded. The module description produced by the compiler, simulator, and/or partitioner (Steps 2-7, col. 10) corresponds to the data model claimed by Applicant, which are then use for both logic synthesis and generating physical placement information (i.e., structural description) (Steps 8-10). As taught in steps 1-7 (col. 9-10), the module description has both functional and logical parameters (i.e., various functionalities or behaviors) as well as the physical parameters (i.e., area, speed, packaging, I/O capabilities, etc.). While Step 3 consults technology files (i.e., several files) as pointed out by Applicant in the interview conducted on 10/12/2001, Applicant's claims recite the generation of signals representative of "a data model", not a file. Applicant should note that as found in any technology files or library files, the circuit module in the technology files or library used for circuit design (i.e., behavioral and/or logic synthesis) are identified by their functionalities or logic parameters (i.e., AND, NAND, Multiplexer, Adder, etc., with corresponding parameters such as the number of inputs, the i/o ports, etc.), as well as physical parameters (i.e., in terms of optimized physical parameters, such as speed,

area, I/O capabilities, as well as the size and relative coordinates of the library object module to be used for instantiation) contains both the logical parameters and physical parameters. In fact, it makes no difference whether there are one or more technology files or library files being consulted, as long as the data model (i.e., module description) generated contains both the logical and physical parameters of the circuit, and the same data model is used for logic synthesis and to generate physical placement information, **Rostoker et al.** meets the language of Applicant's claims as discussed above.

11. As per **claims 21,23-30**, Applicant argued that **Mahmood et al.** like **Rostoker et al.** failed to teach "a data model" that includes both logical synthesis information and physical placement information. The Examiner is not persuaded. Similar to **Rostoker et al.**, the datapath cell instance generated corresponds to Applicant's "a data model" which contains both logical and physical placement information as given in the rejection above. The "separate models" recited by Applicant in support of Applicant's argument, corresponds to the various "at least one model" in the data structure, and not "a data model" to be created or generated as claimed.

12. As per **claims 31-47**, the claims are withdrawn from consideration by the Examiner as directed to non-elected claims by the fact that these claims are directed to an invention that is independent or distinct from the invention originally, which was constructively elected as given above. Accordingly, Applicant's argument for patentability of these claims are mooted.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Aubel et al. (US Patent No. 5,696,693) disclose a method for placing logic functions and cells in a logic design using floor planning by analogy (abstract) wherein the logic functions are derived from the HDL file (col. 10, lines 1-32; Fig. 2) and the cell libraries includes hierarchy, graph tree structure (col. 2, lines 16-58).

Lemche et al. (US Patent No. 5,727,187) disclose a method of using logical names in post-synthesis electronic design automation systems (abstract) including tree structured library of components (col. 2, lines 25-60).

Iwasaki et al. (US Patent No. 5,623,417) disclose a method and apparatus for functional level data interface which permits the unification of functional design automation tools containing tree structured library components (Fig. 3; col. 4, lines 32-53).

Loos et al. (5,487,018) discloses an electronic design automation apparatus and method utilizing a physical information database for interfacing between a datapath cell library and a number of electronic design automation tools (e.g., datapath synthesis too, chip estimator, HDL generation tool, datapath compilation tool), wherein the database includes global parameters applicable to every cell in the datapath cell library and local parameters defining attributes that are associated with individual cells in the datapath cell library (abstract; Fig. 2; col. 3, line 35 to col. 4, line 9).

Sharma et al. (US Patent 5,481,663) disclose a method and apparatus for designing circuit which uses parameterized Hardware Description Language (HDL) modules stored in a library, wherein a datapath synthesizer accesses the library and

assigns values to parameters to form specific implementations of the parameterized HDL modules (abstract; Fig. 16).

Mahmood et al. (US Patent No. 5,519,627) disclose datapath synthesis method and apparatus utilizing a structured cell library (abstract; Fig. 4).

Dutt ("Generic component library characterization for high level synthesis", Proceedings of the Fourth CSI/IEEE International Symposium on VLSI Design, 1991, 4 January 1991, pp. 510) discloses a novel generator-generator language for the definition, generation, and maintenance of generic component description libraries used in high-level hardware synthesis wherein the every high-level synthesis system uses an implicit or explicit generic component library, wherein the library is hierarchically organized into types, generators, components, and instances, allowing the users to add and modify component types easily (abstract; pp. 6-9; Figure 1).

14. The following are other prior arts not relied upon but are considered pertinent to applicant's disclosure. Therefore, Applicants are requested to carefully consider them in response to this Office Action.

Cleereman et al. (US Patent No. 5,960,184) disclose a method and apparatus for providing optimization parameters to an EDA logic optimizing tool, wherein the optimizing parameters for selected circuit modules within a circuit design database may be stored in a single file such that a particular optimization parameter set can be uniquely identified by a search capability of a data processing system (abstract; col. 4, lines 19-56; Figs. 9-15).

Gan et al. (US Patent No. 6,308,309) disclose a place-holding library elements for defining routing paths, wherein the library file contains both physical and logical information (abstract; col. 4, lines 6-28).

Eng (US Patent No. 6,145,117) disclose an electronic design automation system that provides optimization of RTL models of electronic design, having a logic building block (LBB) library with both physical and logical parameters (abstract; col. 9-10).

Ratzel et al. (US Patent No. 5,956,497) disclose a methodology for designing an integrated circuit using a reduced cell library for preliminary synthesis, the cell library containing both logical and physical attributes (abstract; col. 1, line 60 to col. 2, line 18).

Leung (US Patent No. 5,432,707) discloses an automated circuit design using a multiplicity of cells in logic synthesis using a library with both logical and physical parameters (abstract; Fig. 1; col. 3).

Merryman et al. (US Patent No. 5,864,487) disclose a method and apparatus for identifying gate clocks within a circuit design, using a design database that may include a high level behavioral representation, a structural description representation, an optimized structure representation, a physical representation *abstract; col. 8, lines 24-33).

Bold et al. (US Patent No. 6,289,489) disclose a method and apparatus for automatically cross-referencing graphical objects and HDL statements (abstract; Figs. 2, 3A, 3B).

Jones et al. (US Patent No. 5,666,288) disclose a method and apparatus for designing an integrated circuit, wherein a new hybrid library is generated containing both physical and logical or behavioral parameters (abstract; Fig. 4; claim 17).

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is (703) 306-3039. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 5 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith, can be reached at (703) 308-1323. The fax phone number for this Group is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1782.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-3431, (for formal communications intended for entry)

Or:

(703) 308-5841 (for informal or draft communications, please label "PROPOSED" or "DRAFT"'and let the examiner know prior to faxing)

Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

P K
January 27, 2002

MATTHEW SMITH
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